Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.018”**

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**.018”**

**Top Material: Al-Si**

**Backside Material: Au**

**Bond Pad Size: .004” X .004”**

**Backside Potential: COLLECTOR**

**Mask Ref: CP736V**

**APPROVED BY: DK DIE SIZE .018” X .018” DATE: 3/18/19**

**MFG: CENTRAL SEMI THICKNESS .008” P/N: CMPT5401**

**DG 10.1.2**

#### Rev B, 7/1